CLMPTO
11/15/04
CM.

1. An integrated circuit chip with redundant elements, comprising:

a substrate die;

a plurality of microprocessors disposed in said substrate die, each microprocessor having a data interface;

a plurality of cache memories disposed in said substrate die, each cache memory having at least one memory interface for accessing the cache memory; and

a signal bus disposed in said substrate die, said signal bus including a programmable selector circuit for selecting a subset of said plurality of microprocessors to be used for processing information and for selecting a subset of said plurality of cache memories, said selector circuit simultaneously linking the data interface of a first selected microprocessor to a memory interface of a first selected cache memory and linking the data interface of a second selected microprocessor to a memory interface of a second selected cache memory.

2. The integrated circuit chip of Claim 1, wherein the substrate die comprises a conductive silicon substrate having at least one bulk region and at least one silicon-on-insulator region, the cache memories being dynamic random access memories residing on said at least one bulk region and the microprocessors residing on said at least one silicon-on-insulator region.

3. The integrated circuit chip of Claim 1, wherein said signal bus is a broadband signal bus.

4. The integrated circuit chip of Claim 1, wherein said signal bus further comprises at least one active element to regenerate a data signal coupled by the signal bus between the first selected microprocessor and the first selected cache memory.

5. The integrated circuit chip of Claim 1, wherein the chip is a multiprocessor and there are a total of N microprocessors and a subset of N-1 microprocessors is selected for parallel processing by the selector circuit.

6. The integrated circuit chip of Claim 5, wherein there are a total of N cache memories and said selector circuit selects subset of N-1 cache memories for parallel processing.

7. The integrated circuit chip of Claim 5, wherein said cache memories are level-2 cache memory units.

8. The integrated circuit chip of Claim 7, wherein one of said cache memories comprises a cache sized to provide the cache resources of a level-2 cache memory and a level-3 cache memory.

9. The integrated circuit chip of Claim 1, wherein the chip is a multiprocessor and the signal bus couples the microprocessors as a parallel processor.

10. The integrated circuit chip of Claim 9, wherein said plurality of microprocessors includes at least nine microprocessors.

11. The integrated circuit chip of Claim 1 wherein said programmable selector circuit is a multiplexor circuit.

12. The integrated circuit chip of Claim 1, wherein said cache memories include level-2 cache memories and level-3 cache memories and one microprocessor is coupled to one level-2 cache memory and to one level-3 cache memory by the signal bus.

13. A multiprocessor chip, comprising:

a silicon substrate die having at least one bulk region and at least one silicon-on-insulator region, the silicon-on-insulator region including a buried oxide layer residing a preselected distance between an outer surface layer of crystalline silicon;

a plurality of microprocessors, each said microprocessor formed in said at least one silicon-on-insulator region, each microprocessor having a data interface;

a plurality of dynamic random access memory (DRAM) cache memories formed in said at least one bulk region, each cache memory having a memory interface for accessing the cache memory; and

a high bandwidth signal bus formed on said substrate having interconnect wires for linking the data interface of one microprocessor to a corresponding memory interface of one of the cache memories as a parallel processor.

14. The multiprocessor of Claim 13, wherein said signal bus includes a programmable selector circuit for selecting a subset of the components that are utilized by the parallel processor, whereby a defective component may be bypassed, the selected components being chosen from a group consisting of microprocessors, cache memories, and the interconnect wires of the signal bus.

15. The multiprocessor of Claim 13, wherein said cache memories are comprised of trench DRAM memories.

16. The multiprocessor of Claim 15, wherein said buried oxide layer has a thickness of less than 200 nanometers.

17. The multiprocessor of Claim 16, further comprising a layer of ions disposed proximate the interface of the buried oxide layer and the surface layer of crystalline silicon, said ions having a polarity and dose selected to suppress backgate conduction.

18. The multiprocessor of Claim 13, wherein said signal bus includes at least one active element to regenerate a signal coupled between a microprocessor and a cache memory.

19. The multiprocessor of Claim 13, wherein one of the cache memories is a level-2 cache memory.

20. The multiprocessor of Claim 13, wherein one of the cache memories has a data capacity sufficient to provide the function of a level-2 cache memory and a level-3 cache memory.

21. The multiprocessor of Claim 13, wherein the cache memories comprise level-2 cache memories and level-3 cache memories.

22. A multiprocessor chip, comprising:

a silicon substrate die having at least one bulk region and at least one silicon-on-insulator region, the silicon-on-insulator region including a buried oxide layer residing a preselected distance below an outer surface layer of crystalline silicon;

a plurality of microprocessors, each said microprocessor formed in said at least one silicon-on-insulator region, each microprocessor having a data interface;

a plurality of dynamic random access memory (DRAM) level-2 cache memories formed in said at least one bulk region, each level-2 cache memory having a memory interface for accessing the memory; and

a high bandwidth signal bus formed on said substrate die having interconnect wires for linking the data interface of one microprocessor to a corresponding memory interface of one of the level-2 cache memories as a parallel processor, said signal bus including a programmable selector circuit for selecting a subset of said plurality of microprocessors and for selecting a subset of said cache memories to be used for parallel processing, said selector circuit simultaneously linking the data interface of a first selected microprocessor to the memory interface of a first selected cache memory and linking the data interface of a second selected microprocessor to the memory interface of a second selected cache memory, whereby a defective microprocessor or a defective cache memory may be bypassed.

23. The multiprocessor chip of Claim 22, wherein the level-2 cache memories are sized to provide the function of off-chip level-2 cache memories and off-chip level-3 cache memories.

24. The multiprocessor chip of Claim 22, further comprising:

a second plurality of dynamic random access memory (DRAM) cache memories formed in said at least one bulk region, each cache memory of the second plurality of cache memories sized to provide the function of a level-3 cache memory and having a memory interface for accessing the memory, wherein said second plurality of cache memories is simultaneously coupled by said signal bus to the plurality of microprocessors with a first selected microprocessor linked to a first selected one of the second plurality of cache memories and with a second selected microprocessor linked to a second selected one of the second plurality of cache memories.

CLAIMS 25-26. (CANCELLED)